



DLPD3V3LC

#### **3.3V LOW CAPACITANCE BIDIRECTIONAL TVS**

### **Features**

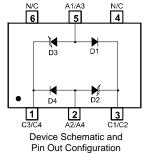
- 330 Watts Peak Pulse Power (tp =  $8x20\mu s$ )
- Transient Protection for data, signal, and  $V_{CC}$  bus to IEC61000-4-2 level 4 (ESD)
- Low Capacitance, typ. <3 pF
- **Bidirectional Configuration**
- Surface Mount Package Ideally Suited for Automated Insertion
- Lead Free By Design/RoHS Compliant (Note 3)
- "Green" Device (Note 4)

### **Mechanical Data**

- Case: SOT-26
- Case Material: Molded Plastic, "Green" Molding Compound, Note 4. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 2
- Ordering Information: See Page 2
- Weight: 0.017 grams (approximate)



Top View



#### Maximum Ratings, Total Device @TA = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Peak Pulse Power (Note 2)	P <sub>pk</sub>	330	W

## Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ ext{ heta}JA}$	286	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

# Electrical Characteristics @T<sub>A</sub> = 25°C unless otherwise specified

Reverse Standoff Voltage	Breakdow V <sub>BR</sub>	n Voltage @ I <sub>T</sub>	Test Current	Max. Reverse Leakage @ V <sub>RWM</sub> (Note 7)	Max. Clamping Voltage @ I <sub>p</sub> = 1A (Note 2)	Max. Clamping Voltage V <sub>C</sub> @ I <sub>PP</sub> (Note 2)	Max. Peak Pulse Current (Note 2)	Typical Total Capacitance
V <sub>RWM</sub> (V)	Min (V)	Max (V)	I <sub>T</sub> (mA)	I <sub>R</sub> (mA)	V <sub>C</sub> (V)	(V)	I <sub>PP</sub> (A)	(pF)
3.3	4.0	_	1.0	0.11	8.0	22	15	2.5

1.  $V_R = 0V$ , f = 1MHz as measured between pins 1 and 3.

2. tp =  $8x20\mu$ s. See figure 2.

Notes:

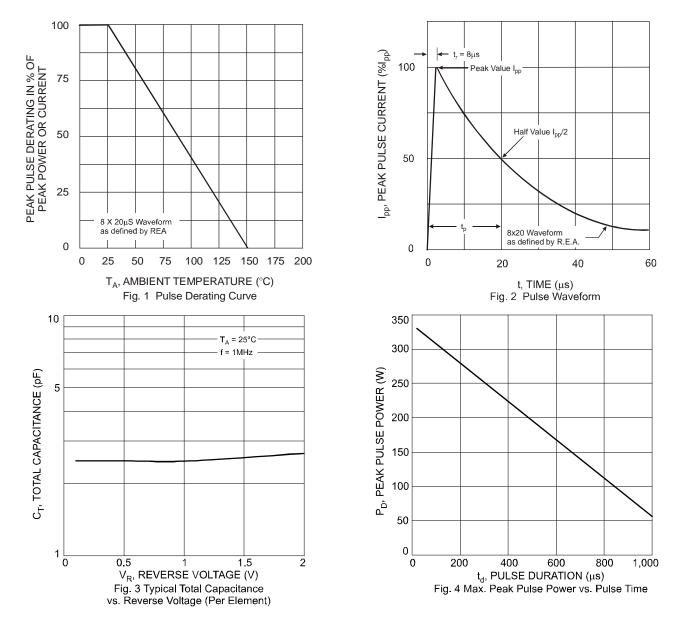
3. No purposefully added lead.

 Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead\_free/index.php.
Device mounted on FR-4 PCB with pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

6. From pin 3 to pin 1, and/or from pin 1 to pin 3.

Short duration pulse test used to minimize self-heating effect. 7





# Ordering Information (Note 8)

Part Number	Case	Packaging
DLPD3V3LC-7	SOT-26	3000/Tape & Reel

Notes: 8. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

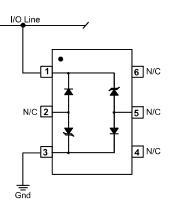
# **Marking Information**

Date Code Key				A02	M.	YM = Y = Ye	Date Cod ear (ex: U	Гуре Markin e Marking = 2007) 9 = Septem	-			
Year	2007	20	08	2009	2010	20	11	2012	2013	20	014	2015
Code	U	١	/	W	Х	Ň	(	Z	А		В	С
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D

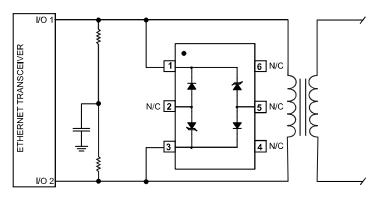


# Typical Applications

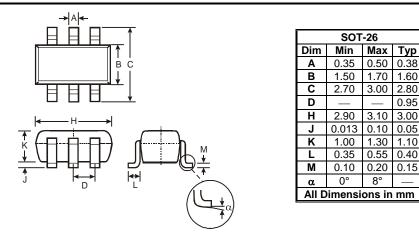
Common-Mode I/O Port Protection



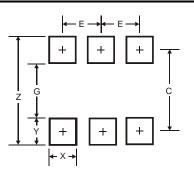
#### Differential-Mode Ethernet Protection



# Package Outline Dimensions



# Suggested Pad Layout



Dimensions	Value (in mm)
Z	3.20
G	1.60
Х	0.55
Y	0.80
С	2.40
E	0.95



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